What is claimed is:

Claim 1. In a software driven emulator comprised of a plurality of modules on printed circuit boards, each of said modules including a processor chip and at least one SDRAM coupled to the processor chip, a maintenance bus coupled to said SDRAM, and a memory controller coupled to said maintenance bus, a method executing bulk data transfers to said SDRAM via said maintenance bus, including the steps of:

transferring data to said SDRAM via said maintenance bus on each clock cycle for a predetermined number of clock cycles in succession;

halting the transfer of data after said predetermined number of data transfers;

initiating a SDRAM refresh cycle after said halting step;

resuming said transferring step upon receipt of a done signal after said refresh cycle.

Claim 2. In a software driven emulator comprised of a plurality of modules on printed circuit boards, each of said modules including a processor chip and at least one SDRAM coupled to the processor chip, a maintenance bus coupled to said SDRAM, and a memory controller coupled to said maintenance bus, a method executing bulk data transfers to said SDRAM via said maintenance bus, including the steps of:

transferring data from said SDRAM via said maintenance bus on each clock cycle for a predetermined number of clock cycles in succession;

halting the transfer of data after said predetermined number of data transfers;

initiating a SDRAM refresh cycle after said halting step;

resuming said transferring step upon receipt of a done signal after said refresh cycle.

Claim 3. A method of executing bulk transfers as in claim 1 including establishing a starting address for said bulk transfer in said memory controller and incrementing said starting address by one on each clock cycle.

Claim 4. A method of executing bulk transfers as in claim 2 including establishing a starting address for said bulk transfer in said memory controller and incrementing said starting address by one on each clock cycle.

Claim 5. A method of executing bulk transfers as in claim 1 wherein a data word is transferred on each clock cycle.

Claim 6. A method of executing bulk transfers as in claim 2 wherein a data word is transferred on each clock cycle.